



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,520	02/24/2004	Liu Huang	CS02-072	8312
7590	09/29/2005		EXAMINER	
STEPHEN B. ACKERMAN 28 DAVIS AVENUE POUGHKEEPSIE, NY 12603			HUYNH, ANDY	
			ART UNIT	PAPER NUMBER
			2818	
			DATE MAILED: 09/29/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/785,520	HUANG ET AL.
	<b>Examiner</b>	<b>Art Unit</b>
	Andy Huynh	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 21 September 2005.

2a)  This action is **FINAL**.                            2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

4)  Claim(s) 1-24 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed.

6)  Claim(s) 1-8, 11-21 and 24 is/are rejected.

7)  Claim(s) 9, 10, 22 and 23 is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on 24 February 2004 is/are: a)  accepted or b)  objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All    b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_  
4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_  
5)  Notice of Informal Patent Application (PTO-152)  
6)  Other: \_\_\_\_\_

## DETAILED ACTION

In the Amendment dated 09/21/2005, Claims 25-37 have been canceled, and Claims **1, 6, 7, 9-11, 13, 19, 20 and 22-24** have been amended. Accordingly, Claims **1-24** are currently pending in the application.

### *Response to Arguments*

Applicant's arguments with respect to Claims **1-8, 11-21 and 24** have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims **1-8, 11-21 and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho et al. (USP 6,486,082 hereinafter referred to as “Cho”) in view of Cheng et al. (US Pub. No. 2005/0153537 filed 01/08/2004 dated 07/14, 2005 hereinafter referred to as “Cheng”).

Regarding Claim 1, Cho discloses in Figs. 3 and 4A-4C, and the corresponding texts as set forth in column 9, line 48-column 10, line 49, a damascene method comprises:

(a) providing a substrate 300;

- (b) depositing a barrier/oxygen doped SiC layer 312 on said substrate;
- (c) forming a first dielectric layer 314 on said barrier/oxygen doped SiC layer;
- (d) forming an opening 317 with sidewalls and a bottom in said first dielectric layer;
- (e) removing said barrier/oxygen doped SiC layer that is exposed at the bottom of said opening;
- (f) depositing a conformal diffusion barrier layer 318 on the sidewalls and bottom of said opening; and
- (g) depositing a metal layer 320 on the conformal diffusion barrier layer that fills said opening.

Cho fails to teach a damascene method comprises depositing a composite barrier/etch stop layer comprised of a lower silicon carbide (SiC) layer. Cheng teaches in Figs. 1-5 that a damascene method comprises depositing a composite barrier layer comprised of a lower silicon carbide (SiC) layer 16 on a substrate 10 (par. [0032]). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teaching of depositing a composite barrier layer comprised of a lower silicon carbide (SiC) layer on a substrate in a damascene process, as taught by Cheng to incorporate into Cho's process to arrive the claimed limitation in order to provide excellent adhesion to the copper layer. Furthermore, the composite barrier provides an excellent etch stop property which prevents oxidation of copper layer during subsequent processes (par. [0038]).

Regarding **Claims 2-3 and 15**, Cho discloses the substrate is comprised of a conductive layer 310 with a top surface and said opening exposes a portion of the top surface of the

conductive layer (Fig. 4B); wherein the conductive layer and the metal layer are comprised of copper (col. 10, lines 32-37).

Regarding Claims **4 and 16**, Cho discloses the diffusion barrier layer is comprised of Ta, TaN, TaSiN, Ti, TiN, W, or WN (col. 10, lines 38-43). Cho and Cheng fail to teach the diffusion barrier layer has a thickness in the range of about 50 to 300 Angstroms. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the diffusion barrier layer having a thickness in the range of about 50 to 300 Angstroms, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding Claims **5 and 17**, Cho discloses all the claimed limitations except for the first, second, and third dielectric layer is comprised of Black Diamond<sup>TM</sup>, CORAL<sup>TM</sup>, fluorine doped SiO<sub>2</sub>, hydrogen silsesquioxane (HSQ), methylsilsesquioxane (MSQ), a fluorinated polyimide, a polyarylether, or benzocyclobutene. Cheng teaches that a dielectric layer may be made of fluorine doped SiO<sub>2</sub>, or benzocyclobutene (par. [0030]). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use a dielectric layer is made of Black Diamond<sup>TM</sup>, CORAL<sup>TM</sup>, fluorine doped SiO<sub>2</sub>, hydrogen silsesquioxane (HSQ), methylsilsesquioxane (MSQ), a fluorinated polyimide, a polyarylether, or benzocyclobutene since it was known in the art that it is good for low-k dielectric material.

Regarding Claims **6 and 19**, Cho and Cheng disclose all the claimed limitations except for the lower SiC layer has a thickness from about 50 to 150 Angstroms and the oxygen doped SiC layer has a thickness between about 50 and 1000 Angstroms. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the lower SiC layer

having a thickness from about 50 to 150 Angstroms and the oxygen doped SiC layer having a thickness between about 50 and 1000 Angstroms, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding Claims **7, 8, 20 and 21**, Cho discloses the barrier/oxygen doped SiC layer is deposited by a PECVD process (col. 9, lines 55-56) that includes an oxygen flow rate from about 20 to 200 standard cubic centimeters per minute (sccm), a helium flow rate of about 700 to 1000 sccm, a trimethylsilane or tetramethylsilane flow rate of about 280 to 350 sccm, a substrate temperature of from 300<sup>0</sup>C to 400<sup>0</sup>C a chamber pressure of 2 to 8 Torr, and a RF power of about 100 to 1000 Watts that is generated with a RF frequency of 13.56 MHz; wherein the substrate temperature is 350<sup>0</sup>C, the RF power is 460 Watts, chamber pressure is 3.5 Torr, the O<sub>2</sub> flow rate is about 30 sccm, the He flow rate is about 800 sccm, and the trimethylsilane flow rate is about 320 sccm to give an oxygen doped SiC deposition rate in the range of 850 to 950 Angstroms per minute (col. 12, line 11-col. 13, line 46).

Regarding Claims **11 and 24**, Cho discloses the method further comprises of treating said oxygen doped SiC layer with an inert gas (N<sub>2</sub>, He, or Ar) plasma before said dielectric layers are formed (col. 9, lines 55-58).

Regarding Claim **12**, Cho discloses the method further comprises of a chemical mechanical polish process to planarize said metal layer (col. 10, lines 46-49).

Regarding Claim **13**, Cho discloses in Figs. 5 and 6A-6G, and the corresponding texts as set forth in column 11, line 6-column 13, line 67, a dual damascene method comprises:

(a) providing a substrate 500 with a conductive layer 502 formed within a first dielectric layer 500, said conductive layer has an exposed top surface that is coplanar with the top surface of said substrate;

(b) depositing a barrier/etch stop layer comprised of a first oxygen doped SiC layer 512 on said substrate;

(c) forming a second dielectric layer 510 on said first oxygen doped SiC layer;

(d) depositing a second oxygen doped SiC etch stop layer 514 on said second dielectric layer;

(e) forming a third dielectric layer 518 on said second oxygen doped SiC layer;

(f) forming an opening comprised of a via 516 that exposes said conductive layer and a trench 520 aligned above said via wherein the via has sidewalls and a bottom and extends through said second and third dielectric layers, second oxygen doped SiC layer, and through the composite barrier/etch stop layer and wherein the trench has sidewalls and a bottom and is formed in the third dielectric layer; and

(g) depositing a conformal diffusion barrier layer 524 on the sidewalls and bottom of said trench and via and depositing a metal layer 526 on said conformal diffusion barrier layer that fills said trench and via.

Cho fails to teach a dual damascene method comprises depositing a barrier/etch stop layer comprised of a lower silicon carbide (SiC) layer on said substrate. Cheng teaches in Figs. 1-5 that a damascene method comprises depositing a composite barrier layer comprised of a lower silicon carbide (SiC) layer 16 on a substrate 10 (par. [0032]). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teaching of

depositing a composite barrier layer comprised of a lower silicon carbide (SiC) layer on a substrate in a damascene process, as taught by Cheng to incorporate into Cho's process to arrive the claimed limitation in order to provide excellent adhesion to the copper layer. Furthermore, the composite barrier provides an excellent etch stop property which prevents oxidation of copper layer during subsequent processes (par. [0038]).

Regarding Claim 14, Cho discloses in Figs. 5 and 6A-6G the method further comprises of forming a cap layer 519 on the third dielectric layer and wherein the trench is aligned above a via that exposes the conductive layer and said trench is formed in the cap layer and third dielectric layer.

Regarding Claim 18, Cho discloses said second and third dielectric layers have a thickness in the range of about 1000 to 10000 Angstroms (col. 11, lines 10-12 and lines 35-37).

#### *Allowable Subject Matter*

Claims 9, 10, 22 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations.

#### *Conclusion*

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Ah

Andy Huynh

09/27/05

Patent Examiner